

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1629	(257/335,339,340,343).CCLS	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:03
L2	498	1 and (trench or recess or sinker or groove)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:57
L3	495	2 and (@ad<"20031017" or @rlad<"20031017")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:57
L4	188	3 and ((Lateral adj dmos) or ldmos or dmos)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:11
L5	3	("4796070"   "5349224"   "5569949").PN. OR ("6548863").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/15 17:26
L6	24	("5445978"   "5672526").PN. OR ("5918137").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/15 17:35
L7	14	("5539238").URPN.	USPAT	OR	OFF	2004/12/15 17:57
L8	719	(lateral adj dmos) or ldmos	USPAT	OR	OFF	2004/12/15 17:57
L9	719	8 and (@ad<"20031017" or @rlad<"20031017")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:57
L10	263	9 and (trench or recess or sinker or groove)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:57
L11	193	10 not 4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/15 17:58
L12	3	("4796070"   "5349224"   "5569949").PN. OR ("6548863").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/15 18:44

L13	20	("20020130358"   "20020177277"   "4605948"   "4754310"   "5233215"   "5323040"   "5436173"   "5449946"   "5539238"   "5592005"   "5679966"   "5710455"   "5801431"   "5844275"   "5861657"   "5874767"   "5885878"   "6040600"   "6069396"   "6307246").PN. OR ("6787872").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/15 18:45
L14	12	("4971926"   "4980306"   "4985368"   "5242841"   "5258332"   "5539238"   "5569949").PN. OR ("5696010"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/15 18:46

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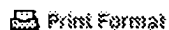
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16 **An intelligent vertical trench DMOS on SIMOX-substrate**

*Vogt, F.; Vogt, H.; Brucker, J.; Zimmermann, C.; Richter, F.;*  
 Power Semiconductor Devices and ICs, 1996. ISPSD '96 Proceedings., 8th  
 International Symposium on , 20-23 May 1996  
 Pages:177 - 180

[\[Abstract\]](#)   [\[PDF Full-Text \(528 KB\)\]](#)   IEEE CNF

17 **A high reliability and low loss 3-phase gate driver IC with a novel soft gate drive circuit for 42V motor generator system**

*Inaba, M.; Sakano, J.; Miyazaki, H.; Iwamura, M.; Maeda, Y.; Mashino, K.; Nagai, Y.; Mori, M.;*  
 Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE  
 15th International Symposium on , 14-17 April 2003  
 Pages:97 - 100

[\[Abstract\]](#)   [\[PDF Full-Text \(374 KB\)\]](#)   IEEE CNF

18 **Robust 80 V LDMOS and 100 V DECMOS in a streamlined SOI technology for analog power applications**

*Merchant, S.; Efland, T.; Haynie, S.; Headen, W.; Kajiyama, K.; Paiva, S.; Shaw, R.; Tachikake, I.; Tani, T.; Chin-Yu Tsai;*  
 Power Semiconductor Devices and ICs, 2002. Proceedings of the 14th International  
 Symposium on , 4-7 June 2002  
 Pages:185 - 188

[\[Abstract\]](#)   [\[PDF Full-Text \(426 KB\)\]](#)   IEEE CNF

19 **Trenched sinker LDMOSFET (TS-LDMOS) structure for high power amplifier application above 2 GHz**

*Cheon Soo Kim; Joung-Woo Park; Hyun Kyu Yu;*  
 Electron Devices Meeting, 2001. IEDM Technical Digest. International , 2-5 Dec.